# Single-Event Upset in the PowerPC750 Microprocessor*

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## I. Introduction

The effects of heavy ions and protons in space on advanced microprocessors are key problems in the design and planning of future spacecraft. Energetic heavy ions can disrupt the functional operation of microprocessors, and in some cases may cause catastrophic effects such as latchup to occur. Radiation tests of microprocessors are difficult and costly. Only a few microprocessors have been subjected to radiation tests and, because of the rapid pace of the commercial processor market, those results are for devices with larger feature sizes and higher operating voltages than current devices [1-6].

Single-event tests were done to provide estimates of upset rates in various space applications, including earth orbiting, deep space and planetary exploration missions as well as to determine whether new failure or upset modes occur in new, advanced processors.

In this paper we report results of single-event tests of the PowerPC750 from Motorola and IBM, which are identical designs which are manufactured with advanced processes that uses a minimum feature size of 0.29 and 0.28 μm, respectively. This report includes test results for all program-visible PowerPC750 registers, the L1 caches, the L2 tags, and the page table buffer as well as overall results for processor functionality. A series of tests was done using two different types of radiation sources: energetic protons, which have sufficient range to penetrate the packaging material of the PowerPC750, and heavy ions, which have limited range, and require tests in vacuum on specially prepared units that have been thinned so that the ions can penetrate to the front side of the die using irradiation from the back.

The test approach was based on commercially available development boards that provide much of the hardware required to make the processor operational. A simplified operating system was used in conjunction with the test boards. A number of elementary software programs were written to enable errors in various sections of the processor to be distinguished. Table I lists various registers and features of the PowerPC750 that were considered in the software and testing.

TABLE 1

| Abbreviations | Description | # of bits |
|---|---|---|
| GPR | General Purpose Registers | 1024 |
| FPR | Flotating Point Registers | 2048 |
| SR-SPR | Special Purpose Registers | 2560 |
| Data Cache Data Bits | *self-explanatory* | 256K |
| Data Cache Tags & Flag | Cache Addresses | 20K |
| Instruction Cache Data Bits | *self-explanatory* | 256K |
| Instruction Cache Tags & Flag | Cache Addresses | 20K |
| TLBs | Page Table Cache | 1024 lines |
| L2 Cache Tags & Flag | L2 Cache Addresses | 40K |

## II. Experimental Method

We used Motorola's PowerPC evaluation board known as "Yellowknife" as a test platform. This board was chosen because it eliminates the large engineering effort required to design a custom test board for the processor and also provides a very basic internal operating system that eliminates the many layers of code in more advanced operating systems. This provides far better diagnostic information and control of processor information flow. The Yellowknife has a small daughter card for the processor and cache with no active components underneath which is important for penetrating proton irradiation (this allowed us to shield other components on the board during proton tests, assuring that the measured response was entirely due to effects within the processor). The Yellowknife board has many features associated with a Personal Computer, including PCI and ISA slots, floppy and IDE disk controllers, keyboard connection and multiple I/O ports. It comes with a simple monitor/debugger that Motorola has dubbed DINK. DINK communicates over a bi-directional serial port to a computer terminal. The other external communication provided on the

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Yellowknife is a JTAG port (JTAG is an industry standard, boundary scan interface). An Agilent Technology 5900B JTAG probe was used for our tests. It was then possible to interrogate the processor even after unexpected events occurred such as operational errors during irradiation.

Two main test methodologies were developed: (1) the "do nothing with strip chart" method and (2) the "pin wiggler" method. In the "do nothing with strip chart" method the processor is programmed to perform a simple instruction in a small infinite loop and write a register snapshot to a strip chart in the physical memory every half second. The "do nothing" loop is a one word instruction that always branches back to itself. This minimizes processor activity and reduces the number of internal operations, thereby making the operation susceptible to errors in only a few internal locations. Even program counter upsets are trapped (via a "system call" instruction) and counted and the "do nothing loop" is re-energized. After the irradiation has ended, an external interrupt triggers a subroutine to count state changes in internal registers or the data cache.

In the "pin wiggler" method, the processor is programmed to perform a self-inspection of its internal registers, and to toggle an address pin if an error is found in these registers. The "pin wiggler" method has the advantage of providing active, continuous feedback to the experimenter during the irradiation while the "do nothing" method is essentially blind until the test run has been completed. A set of external hardware counters was used to monitor the wiggling pins on the Yellowknife board to determine if any changes occurred during the irradiation. The lines were coded to indicate (a) whether the main software loop was still functioning properly; (b) if an upset had just been detected; and (c) whether a coded internal timer, that activated an interrupt, continued to function.

More complex methods were required to examine errors in the L1 data and instruction caches. The two types of caches were initialized in specified conditions prior to irradiation. Both caches were then disabled. Then a clearly recognizable pattern *designed to be distinctly different from the content of the cache* was placed in the external memory space covered by the caches. Verification of the cache contents was done by comparing the cache contents after irradiation. Verification of the instruction cache was only possible using the JTAG interface, examining the instruction cache to determine its contents. Tag upsets (as well as upset of the data valid flag) were detected by monitoring for the distinctly different pattern. The tag and data valid upsets were thus distinguished and counted separately from upsets of the data bits themselves.

Additional test programs were developed that used the floating point unit within the processor. Those tests were done in order to determine whether transient logic errors within the floating point unit would cause the error rate to increase. This provided an indirect method to evaluate transient logic errors because the floating point unit contains a very large array of combinational logic.

Proton tests are far more straightforward than tests with heavy ions because the tests can be done in air, without any need for package modification or vacuum chambers. Proton tests with energies above 65 MeV were performed at the Indiana University Cyclotron Facility. Tests at lower energies were done at the UC Davis cyclotron.

Heavy-ion testing is far more complicated than proton testing because the "flip-chip" design of the PowerPC750 does not allow the device to be "delidded" in the usual sense without destroying the pad and bonding connections. The limited range of most heavy-ion facilities does not allow them to penetrate the package. Although it is possible to use ions with extremely energetic beams to overcome this problem, such facilities are extremely costly and difficult to schedule. We did tests with more conventional facilities by milling away part of the back surface of PPC750, reducing the thickness of the die from 712 μm to 50-200 μm. Several thicknesses were used to address the concern that if the die was too thin, it might affect the charge collection. With the thinner dice, heavy ions from a low energy accelerator are able to penetrate the active region. The upset mechanism requires penetration of the ion beyond the top surface of the die. The Texas A&M accelerator was used because they provide ions much longer range than other available heavy ion facilities. These tests had to be done by placing the entire Yellowknife board and JTAG probe in the vacuum system. The processor and other components on the board must dissipate considerable amounts of power, and tend to overheat when used in this way. The data presented here was collected by allowing time for the processor to cool between successive irradiation. A thermocouple was used to measure temperature increases during the time that the device operated within the vacuum system.

## III. Proton Test Results

The first tests that were done with protons were successful in identifying errors in registers, but the test results were occasionally disrupted by program "hangs". This was partly due to the implementation method used in the initial tests, which effectively relied on successful processor operation to identify internal errors. Program "hangs" were also observed in earlier tests of other microprocessor types [1-6], and are difficult to deal with.

One way to deal with the "hang" problem was to use the "pin wiggler" method to continually monitor status and errors during each run. Figure 1 shows an example.

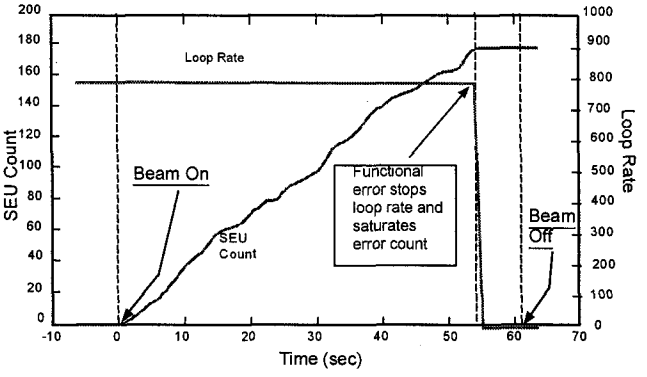


Figure 1. Error count accumulation and processor status information during a test run using the "pin wiggler" method.

In this figure, errors develop in a nearly linear way as the test progresses. This shows that there are no significant error bursts, and that the error event rate is nominally proportional to the incremental proton fluence. However, near the end of the test run the processor "hangs", which is evident by the loop counter response as well as sudden saturation of the errors. Although this approach does not eliminate "hangs" it allows valid data for part of a test run to be extracted from the run, as well as providing information about error propagation from the processor.

With this approach, we were able to measure the error rate for different types of internal registers at various proton energies. Figure 2 shows the results for the floating-point registers, with logic "1" stored; thus, the errors represent transitions from "1" to "0". The threshold energy is below 20 MeV, the lowest energy tested.

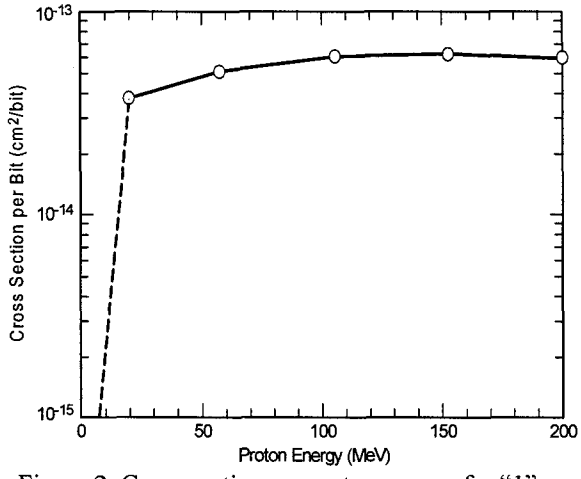


Figure 2. Cross section vs. proton energy for "1" upset to "0" transition of floating point registers in the PowerPC750

The cross section for "1" to "0" errors saturated at about $10^{-13}$ errors-cm$^2$/p-bit. For the opposite transition ("0" to "1"), the error rate was consistently lower by about a factor of 3. This asymmetry is not unusual for minimum-area, statically-implemented registers.

Test results for the general-purpose and special-registers were very similar to the results obtained for the floating-point registers, with nearly the same saturation cross section. However, the threshold energy for the general-purpose registers and special-purpose registers were slightly higher with some difference in the curve shape.

Results for the data cache bits were significantly different, as shown in Figure 3. First, the decrease in cross section occurs at energies that are considerably lower than that of the other registers. The 20 MeV lower limit of the UC Davis facility prevents characterization of the low energy response of the

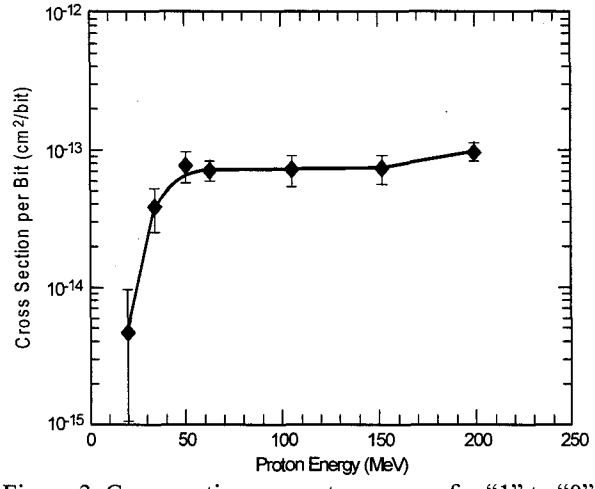


Figure 3. Cross section vs. proton energy for "1" to "0" transition of the data cache bits in the PowerPC750 processor. Note that the statistical error bars are smaller than the plot symbol.

cache. The saturation cross section is nearly a factor of two lower. The threshold behavior is likely the result of implementing dynamic storage to reduce the bit area (there are 256K bits in each L1 cache). Thus, the critical charge required for upset is reduced. The lower saturation cross section is probably due to reduced bit area.

The data cache tags and the "invalid" flag had similar responses during proton tests. The instruction cache results indicate that is also had a similar response to protons.

It is also interesting to compare our results for the 0.29 μm PowerPC750 with older results for the PowerPC603 [5] which has a feature size of 0.4 μm and represents the previous generation of advanced microprocessors from Motorola. The register error

rate for the PPC750 is about a factor of three lower than that of the PPC603, with comparable energy thresholds for the two types of processors. Thus, the increased speed and higher density of the PPC750 does not appear to have increased the sensitivity of the registers to upset from protons.

## IV. Heavy Ion Test Results

As discussed in the Introduction, heavy ion tests are far more difficult to do with advanced processors because of the difficulty of getting ions to penetrate the flip-chip package assembly. Heating of processors during the test within the vacuum system is also a problem. The PPC750 dissipates 4-5 W during normal operation at the highest clock rate, which is considerably lower than the power dissipation of most other high-speed processors. We used a heat sink on the package to provide cooling to the device during tests and monitored the device temperature with a thermocouple.

Heavy ion test results for register errors showed that Figure 4 shows the dependence of the cross section on LET for the special-purpose registers (results for other types of registers exhibited similar but not identical behavior). The cross section increased rapidly from about $10^{-9}$ cm$^2$/bit to approximately $10^{-7}$ cm$^2$/bit at higher LET values, consistent with the PPC603 results of Bezerra, et al.[5] The threshold LET is 3-4 MeV-cm$^2$/mg, about a factor of 2 higher than the PPC603 [5]. Thus, the increased scaling and decreased internal operating voltage of the PPC750 have apparently decreased SEU sensitivity.

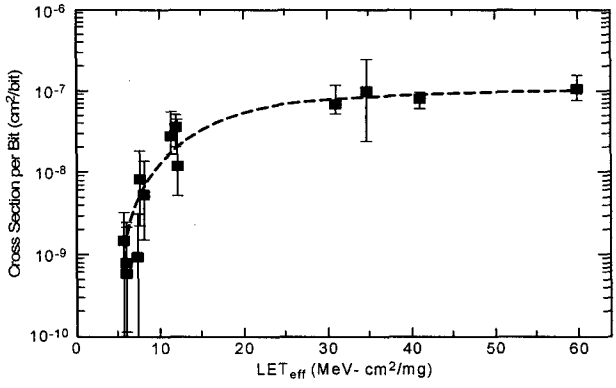


Figure 4. Heavy-ion upset cross section for special-purpose registers in the PowerPC750 for "1" to "0" upsets.

The data in Figure 4 are for "1" to "0" transitions. The cross section for transitions from "0" to "1" is a factor of three lower, consistent with the proton test results.

There are many different data points in this curve, with a number of different test conditions and two different test methods. Several different parts were used, with thicknesses of 50, 100 and 200μm. The LET at the device surface is corrected for the decrease in beam energy as the ions traversed the device. There is good agreement in the results for the different devices after the transport correction.

A more detailed look at upset cross section results for devices with different final thicknesses after "back milling" is shown in Figure 5. This appears to validate irradiation from the back as an experimental approach, although in this case we do not have irradiation data from the top for comparison.

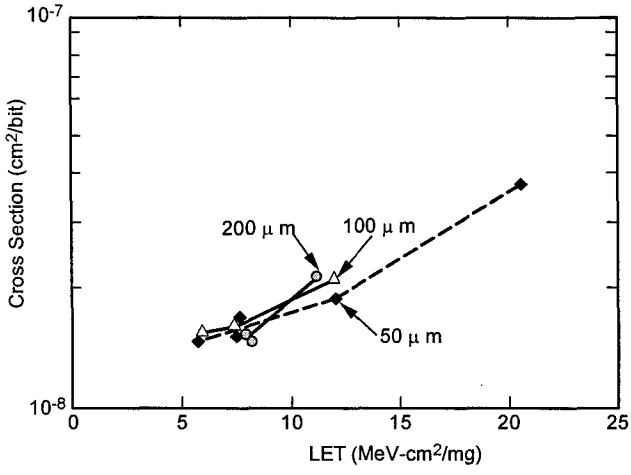


Figure 5. Comparison of cross section data for devices with different die thickness after corrections were made for the effect of transport through the die on particle LET.

## V. Conclusions

These results show that single-event upset susceptibility in advanced commercial processors is actually somewhat improved compared to an earlier generation of the same processor family, allowing them to be used in space applications where occasional malfunctions can be tolerated. Although comparisons of register upset rates are a useful way to examine single-event susceptibility, the more difficult issue is how frequently more complex malfunctions of the processor occur, and how they can be detected and corrected when more complex operating systems are used. Interestingly, these "hangs" were much less frequent than seen for Pentium processors [6], which may be due to the more basic operating system in the Yellownknife board. Heavy ion tests of these complex parts were done using irradiation from the back of the die on mechanically thinned samples. The test results show that consistent cross section values can be obtained by comparing the effective LET of samples with different thicknesses, validating the back irradiation test approach.

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